SPACE VECTOR PWM MODULATOR FOR PERMANENT MAGNET MOTOR DRIVE

CROSS-REFERENCE

[0001] This application is based on and claims priority of U.S. Provisional Application Serial No. 60/418,733 filed October 15, 2002, incorporated by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The invention relates to a motor drive, and more particularly to a drive method and system for a permanent magnet surface-mount (PMSM) motor utilizing a space-vector PWM modulation scheme.

2. Description of the Related Art

[0003] Three-phase motor drives utilizing inverters are well known in the industry. Typically a DC bus supplies switched power to different phases of an AC motor. For supplying switching commands and sequences to the inverter, sensorless vector control is achieving wide attention. Sensorless control eliminates speed, flux and torque sensors and replaces them with DSP-based estimation based on the measured terminal voltages and currents. Thus, the cost of the drive is reduced and reliability is enhanced. A DSP-based motor drive of background interest is described in the present inventor's U.S. Applications Serial No. 60/465,890 filed April 25, 2003; and Serial No. 10/294,201 filed November 12, 2002, incorporated by reference. However, the estimation algorithms tend to be complex, particularly at low frequencies.

[0004] Space-vector pulse-width modulation (SVM) has become a popular form of pulse-width modulation (PWM) for voltage-fed converter drives because of its superior harmonic quality and extended linear range of operation. SVM arrangements of background interest are described in Serial No. 10/402,107 filed March 27, 2003, incorporated by reference.

[0005] However, one problem of SVM is that it requires complex on-line computation that usually limits its operation to switching frequencies of up to several kilohertz (e.g. about 10

kHz). Switching frequency can be extended by using high-speed DSP and simplified algorithms including lookup tables (LUT). Power semiconductor switching speeds, particularly in IGBT's, have been improving dramatically. However, the use of LUT's, unless very large, tends to reduce pulse-width resolution.

SUMMARY OF THE INVENTION

[0006] The present invention avoids the intensive calculations such as arctan and square root functions and lookup tables in the conventional space vector PWM modulation scheme. An algorithm structure is proposed for the implementation of a versatile space vector PWM scheme, which can generate both 3-phase and 2-phase SVPWM without intensive math functions or lookup tables. This structure supports overmodulation, symmetrical PWM and asymmetrical PWM modes.

[0007] The invention implements a versatile 2-level space vector PWM (SVPWM) modulator, which allows 3-phase and 2-phase modulation algorithms to be implemented in a common algorithm structure. The implementation utilizes mainly decision logic and does not require any intensive math functions such as arctan, sine, cosine and/or square root functions. The algorithm provides overmodulation, symmetrical and asymmetrical mode capabilities.

[0008] The invention provides a space vector pulse-width modulator and a method implemented by the modulator.

[0009] According to an aspect of the invention, a space vector pulse-width modulator (SVPWM) may comprise a precalculation module which accepts Ua and Ub modulation indexes and in response thereto, outputs modified Ua and Ub information.

[0010] According to another aspect of the invention, a SVPWM may comprise a sector finder having a U module which receives Ua or modified Ua information and outputs a U sector; and a Z module which receives the U sector and Ub or modified Ub information and outputs a Z sector; said U sector and said Z sector being 2-phase control signals for implementing 2-phase modulation.

[0011] According to another aspect of the invention, a SVPWM may comprise, for 3-phase modulation, an active vectors calculation module and an assign vectors module which receive Ua and Ub or modified Ua and Ub information and a U sector, and which calculate active vectors for

3-phase modulation; a zero vector selector which receives said Z sector and calculates zero vectors for 3-phase modulation; and a PWM counter block which receives said active vectors and zero vectors and outputs 3-phase control signals for implementing 3-phase modulation.

[0012] The PWM counter block preferably has a symmetrical PWM mode, an asymmetrical PWM mode, or both.

[0013] The SVPWM may further comprise a rescale and overmodulation module which receives duration information corresponding to vectors and in response thereto, detects the occurrence of overmodulation. Overmodulation is preferably detected in response to a negative zero vector time. The module may respond to overmodulation by clamping a zero vector time to zero and rescaling active vector times to fit within a PWM cycle.

[0014] Said rescaling may restrict a voltage vector to stay within hexagonal boundaries on the space vector plane, while preserving voltage phase.

[0015] According to another aspect, the invention provides a method carrying out at least the steps outlined above.

[0016] Other features and advantages of the present invention will become apparent from the following description of embodiments of the invention which refers to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWING(S)

[0013] Figure 1 is a diagram illustrating 3-phase and 2-phase modulation schemes.

[0014] Figure 2 is a structural block diagram of the versatile space vector PWM modulator.

[0015] Figure 3 shows the precalculation and sector finder blocks of Figure 2 in more detail.

[0016] Figure 4 shows the active vectors calculation block of Figure 2 in more detail.

[0017] Figure 5 shows the rescale and overmodulation block of Figure 2 in more detail.

[0018] Figure 6 is a diagram illustrating overmodulation.

[0019] Figure 7 shows the zero vector selector block of Figure 2 in more detail.

[0020] Figure 8 shows the sequence of states.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

[0021] Following is a description of an example of the PWM scheme.

[0022] 3-phase and 2-phase PWM modulation schemes are shown in Fig. 1. The Volt-sec generated by the two PWM strategies are identical. However, with 2-phase modulation, the switching losses can be reduced significantly, especially when high switching frequency (>10kHz) is employed.

[0023] Fig.2 shows the structural block diagram of the Versatile Space Vector PWM modulator. The design of each block will be described below in more detail. The features of this SVPWM are:

- Implementation does not require Arctan, Sine, Cosine or Square root functions
- Accepts rectangular inputs Ua and Ub (can easily interface to most Vector Controllers)
- Zero vectors can be selected as desired
- Simple overmodulation scheme by zero vector time clamping
- Automatic Symmetrical and Asymmetrical mode generation by half PWM cycle updating.

[0024] Fig. 3 shows details of the calculations in the Precalculation and Sector Finder blocks of Fig. 2. The input of the SVPWM accepts modulation indexes Ua and Ub (orthogonal) and the outputs are U_Sector and Z_Sector (which are used for 2-phase modulation only). The sector regions are defined in Fig. 3. The sector finder is entirely based on decision logic, which provides ease of implementation for a digital hardware platform such as an FPGA.

[0025] The outputs are U_Sector and Z_Sector, which are defined as follows:

[0026] U_Sector

1 0 <= theta < 60

2 60 <= theta < 120

3 120 <= theta < 180

4 180 <= theta < 240

5 240 <= theta < 300

6 300 <= theta < 360

Z_Sector

A -30 <= theta < 30

B 30 <= theta < 90

C 90 <= theta < 150

D 150 <= theta < 210

E 210 <= theta < 270

F 270 <= theta < 330

[0027] Fig. 4 shows details of the calculation in the Active Vectors Calculation block of Fig. 2. This calculation is mainly assignment. There is no intensive calculation involved.

[0028] Fig. 5 shows the Rescale and Overmodulation block. Overmodulation is detected by a negative value on the calculation of zero vector time (T0_Cnt_Scl). By clamping the zero vector time to zero (if negative) and rescaling the active vector times to fit within the PWM cycle, overmodulation can be handled easily. This rescaling restricts a voltage vector to stay within the hexagon limit on the Space Vector plane (Fig.6). The magnitude of the requested voltage is restricted to the maximum possible voltage limit (the hexagon in Fig. 6). However, the voltage phase is always preserved.

[0029] Fig. 7 shows the details of the zero vector selector block. In Fig. 1, for the first half of PWM cycle (PWM_CNT_MAX) there are two zero vector states for 3-phase modulation and one zero vector state for 2-phase PWM. For 3-phase PWM, the first zero vector state is always V7 and the second is V8. However, for 2-phase PWM, the one zero vector state can be V7 or V8 depending on where the voltage vector locates (Z_Sector). Therefore a zero vector selector is implemented to handle various zero vector possibilities.

[0030] The PWM counter block in Fig. 2 implements the PWM gating commands (PhaseU, PhaseV, PhaseW). The block has a state sequencer which steps through the different states (VEC1 to VEC4 shown in Fig. 1). The VEC1 and VEC4 states both implement zero vectors and VEC2 and VEC3 implement active vectors. For every half PWM cycle, the inputs to the PWM counter block are sampled once, which allows asymmetrical PWM mode operation to be implemented inherently without any reconfiguration.

[0031] For 3-phase modulation, the state sequencer implements VEC1 - VEC2 – VEC3 – VEC4 –VEC4 –VEC3 – VEC2 –VEC1 as shown in Fig.8. In the VEC1 state, the first zero vector will be implemented based on T0_Vec_1 and T0_Cnt. There are three PWM counters, two for

active vectors and the third for the two zero vectors. For a 2-phase PWM modulation scheme the state sequencer does not enter state VEC4 (VEC1- VEC2 –VEC3 –VEC3 –VEC2-VEC1).

[0032] There are two active vectors present for each half PWM cycle. The "Assign Vector" block (Fig. 2) determines which of the two active vectors should be used to implement the states VEC2 and VEC3. The zero vector time (T0_Cnt) is half when 3-phase PWM is selected.

[0033] Definitions

Ua – Alpha axis modulation

Ub – Beta axis modulation

U_Sector – Sector number 1 to 6 as shown in Fig. 3 (each sector 60 Deg)

Z_Sector – Sector number A to F as shown in Fig. 3 (each sector 60 Deg)

Ta_Cnt_R – Normalized time duration for active vector A

Tb_Cnt_R – Normalized time duration for active vector B

Ta_Vec_R – Active vector A (V1 to V6) for formation of command modulation vector

Tb_Vec_R – Active vector B (V1 to V6) for formation of command modulation vector

T0_Vec_1 – Zero vector (V7 or V8) being used in state VEC1

T0_Vec_2 – Zero vector (V7 or V8) being used in state VEC4

Ta_Cnt_Scl – Rescaled version of Ta_Cnt_R

Tb_Cnt_Scl – Rescaled version of Tb_Cnt_R

T0_Cnt_Scl – Rescaled version of zero vector normalized time

Ta_Cnt – Counter time duration for state VEC2

Tb_Cnt – Counter time duration for state VEC3

T0_Cnt – Counter time duration for state VEC1 and VEC4

Ta_Vec – Vector being used in state VEC2

Tb_Vec – Vector being used in state VEC3

Two_Phs_Pwm – Select between 3-phase or 2-phase modulation

Z_Mode – 2-phase modulation zero vector selection mode

[0034] Although the present invention has been described in relation to particular embodiments thereof, many other variations and modifications and other uses will become apparent to those skilled in the art. Therefore, the present invention is not limited by the specific disclosure herein.